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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,058	10/23/2003	Yun-Hee Cho	3364P145	1553

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EXAMINER	
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ART UNIT	PAPER NUMBER
2613	

MAIL DATE	DELIVERY MODE
07/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,058	CHO ET AL.	
	Examiner	Art Unit	
	Thi Q. Le	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,9 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,9 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is in response to Applicant's amendment filed on 5/10/2007. **Claims 1-2, 4-7, 9-10** still pending in the present application.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claims 1, 2, 4 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bordogna et al. (US Patent #6,683,855)** in view of **Blair et al. (US Patent 7,028,241)** and further in view of **Little et al. (US Patent # 4,268,722)** and further in view of **Perkins et al. (US PGPub 2004/0156325)**.

Consider **claim 1**, Bordogna et al. clearly show and disclose; an optical transmission system including a plurality of layers, the system comprising: a digital wrapper interrupt processor for processing an interrupt signal generated from the digital wrapper according to monitoring of the received signal (read as, checking parity bits for error, so that forward error correction can be enable or disable) (figure 8; column 9 lines 25-31); a defect and maintenance signal detector for determining whether or not the received signal has a defect (read as, error) and determining whether or not the received signal requires maintenance under the control of the digital wrapper interrupt processor (read as, when error is detected and forward error correction is enable, the data is stored and FEC correction bits are calculated to determine the location of the errors) (figure 8; column 9 lines 32-36); a defect and maintenance signal processor for, when a defect is detected by the defect and maintenance signal detector or is cancelled, processing the defect (read as, correcting the error as shows in block 808) (figure 8; column 9 lines 32-40).

Bordogna et al. fail to disclose, an optical transponder having a digital wrapper, the optical transponder operates to execute maintenance of a received signal in the optical

transponder; and a digital wrapper controller for controlling the digital wrapper according to the processing result of the defect and maintenance signal processor; and wherein the plurality of layers includes at least one among an optical transport unit layer, an optical data unit layer, and an optical payload unit layer, and the digital wrapper interrupt processor sets a defect mask for each layer and processes an interrupt of each layer when the defect mask therefor is true.

In related art, Blair et al. disclose, an optical transponder (read as, output edge component 244; figure 12) having a digital wrapper (read as, frame structure; figure 5), the optical transponder operates to execute maintenance of a received signal in the optical transponder (read as, the output edge component 244 performs FEC decoding and correcting errors in data frame; column 13 lines 63-65); and a digital wrapper controller (read as, FEC/FDC byte allocator 252; figure 12) for controlling the digital wrapper according to the processing result of the defect and maintenance signal processor (read as, the output edge component 244 detects error in the data, "error data" are generated. The error data is process by the FEC/FDC byte allocator 252; new parameters for transmission, in order to reduce error within the data; figure 12; column 14 lines 10-25) (figure 12; column 13 line 63 – column 14 line 35); and wherein the plurality of layers includes at least one among an optical transport unit layer, an optical data unit layer, and an optical payload unit layer (read as, the data frame used by Blair is structured as set forth in ITU-T Recommendation G.709; thus, although not indicated the data frame structure includes at least one, an OTU layer, an ODU layer, and an OPU layer; column 1 lines 25-65).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teaching of Blair et al. with Bordogna et al. Since hardware is

necessary to execute the process described by Bordogna et al. Also, a device for controlling a digital wrapper according to the error detected is necessary so that errors can be reduces.

Perkins clearly disclosed a conventional digital wrapper frame structure set forth in G.709. Shown in figure 2, is a wrapper frame structure wherein it includes ODU layer, OPU layer, and OUT layer.

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Perkins with Bordogna as modified by Blair. Since Perkins disclosed clearly the conventional framing structure of a digital wrapper set forth in G.709.

In related art, Little et al. disclose a telephone communications system. Wherein incoming pulse-code-modulation (PCM) channels (read as, the equivalent of the plurality of layers within the digital wrapper) can be mask using a mask bit. The purpose of the mask bit is for selectively masking particular bits of the selected PCM channel/s. Such, that those bits that are masked are ignore for further processing (abstract; column 19 lines 64-68; column 20 lines 1-8; column 21 lines 60-65; and claim 14) (read on limitation, the digital wrapper interrupt processor sets a defect mask for each layer and processes an interrupt of each layer when the defect mask therefor is true).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teaching of Little et al. with Bordogna et al. as modified by Blair et al. Since adding the ability to selective executing error detection and correction for particular signals increase Network management flexibility. Also it would increase processing speed of a network, since some signal might not need error protection; thus, the ability to ignore (or

exclude) those signals from error detection and correction process would increase the overall speed of the network.

Consider **claim 2, and as applied to claim 1 above**, Bordogna et al. as modified by Blair et al. further disclose; when the digital wrapper interrupt processor detects an interrupt with respect to the received signal from the digital wrapper and determines that the received signal has a defect (read as, when performing parity check and errors are found within the data), the digital wrapper interrupt processor calls the defect and maintenance signal detector to allow it to detect the defect (read as, data is stored and FEC correction bits are calculated to determine the location of the errors) (Bordogna et al.; figure 8; column 9 clines 10-25).

Consider **claim 4, and as applied to claim 1 above**, Bordogna et al. as modified by Blair et al. further disclose, wherein a signal that is received and transmitted by the optical transponder has a structure that maps a client signal to a payload and includes an error correction code and an overhead (figure 2, shows a frame structure that includes, an overheard section which carries a forward error correction section, and a payload section (Bordogna et al.; figure 2).

Consider **claim 7**, it is rejected for the same reason as claim 1 above. Note, Bordogna et al. as modified by Blair et al. discloses both, devices and methods on with the devices can be set up to execute, in order to detect errors within the data and perform error correction. Further, the optical transport network frame structure as disclosed by Blair conforms to ITU-T G.709, which mean the transport network has multi layers.

Consider **claim 9, and as applied to claim 7 above**, claim 9 is rejected for same reasoning as claim 1 above, see the explanation in claim 1. Bordogna et al. as modified by Blair et al. and modified by Little et al. and further modified by Perkins clearly disclose the process of

using a mask bit (read as, setting a defect mask for each later), such that, only a selected number of signals are subject to further signal processing (read as, processing an interrupt of each layer when the defect mask therefor is true), while other signals are ignore (Little et al.; abstract; column 19 lines 64-68; column 20 lines 1-8; column 21 lines 60-65; and claim 14).

7. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Bordogna et al. (US Patent #6,683,855)** in view of **Blair et al. (US Patent 7,028,241)** and further in view of **Little et al. (US Patent # 4,268,722)** and further in view of **Perkins et al. (US PGPub 2004/0156325)** and further in view of **Tezuka (US Patent # 7,028,231)**.

Consider **claim 5, and as applied to claim 4 above**; Bordogna et al. as modified by Blair et al. and modified by Little et al. and further modified by Perkins, disclosed the invention as described above; except for, a transmitter information providing part for providing information required to be delivered to a receiving side through the overhead of the transmitted signal; and a receiver information providing part for providing an expected value of information required to be received through the overhead.

In related art, Tezuka discloses a performance monitoring for optical transmission system. Wherein, one of the steps for error detection and correction method includes using parity calculations and comparisons. Parity is calculated and included in the overhead portion of each frame before transmission. When receiving a frame, parity is again calculated and compared with the parity stored in the overhead portion of each frame. If the two parities are not the same, a disparity flag is set (abstract; figure 3; column 4 lines 55-65 and column 1-15).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teaching of Tezuka with Bordogna et al. as modified by Blair et al.

Since using parity checking is a simple and fast method for indicated occurrences of errors within the received data. Thus, using parity checking can speed up signal processing process.

8. **Claims 6 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bordogna et al. (US Patent #6,683,855)** in view of **Blair et al. (US Patent 7,028,241)** and further in view of **Little et al. (US Patent # 4,268,722)** and further in view of **Perkins et al. (US PGPub 2004/0156325)** and further in view of **Sheridan et al. (US Patent # 6,725,032)**.

Consider **claim 6 and as applied to claim 1 above**, Bordogna et al. as modified by Blair et al. and modified by Little et al. and further modified by Perkins, disclosed the invention as described above; except for, a remote information display for displaying presence/absence of a defect and the quantity of BIP-errors according to the result of the defect and maintenance signal processor; a defect correlation reporting part for finding the cause of the defect to report it; and a performance monitoring part for monitoring a performance value of the received signal to report it.

In related art, Sheridan et al. disclose a cell network management system. Wherein, the alarm reporting system and configuration error unit display any occurrences of errors to the user, including the numbers of errors. Errors are identified, so that for each error, the severity, error type (read as, cause of defect), and a description of the error is display to the user. Also, within the configuration data and alarms elements 312, has performance monitoring systems (figures 3, 6, 8; column 5 lines 27-35; column 8 lines 34-42; column 9 lines 65-67).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teaching of Sheridan et al. with Bordogna et al. as modified by Blair

et al. Because the user can manage/troubleshoot the network better and more efficiently when he/she know the cause of the error and the performance of the network.

Consider **claim 10, and as applied to claim 7 above**, see claim 6. Bordogna et al. as modified by Blair et al. and further as modified by Sheridan et al. clearly disclose the apparatus and method of displaying errors, error rate, cause of error and performance monitoring.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 7, 5, 6, 9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thi Le whose telephone number is (571) 270-1104. The Examiner can normally be reached on Monday-Friday from 7:30am to 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rafael Perez-Gutierrez can be reached on (571) 272-7915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Thi Le

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER